CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**A070VW08 V0**
CUSTOMER APPROVED	**Title :** **Name :**

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.2)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.2)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.2)**
- ☐ **CUSTOMER REMARK :**

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Product Specification

7" COLOR TFT-LCD MODULE

MODEL NAME: A070VW08 V0

Model Name：	A070VW08 V0
Planned Lifetime:	From 2010/Jul To 2011/Dec
Phase-out Control:	From 2011/Jul To 2011/Dec
EOL Schedule:	2011/Dec

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/04/02	All	First Draft.
0.1	2010/04/28		
0.2	2010/06/07	All	Revised EE characteristics

Contents

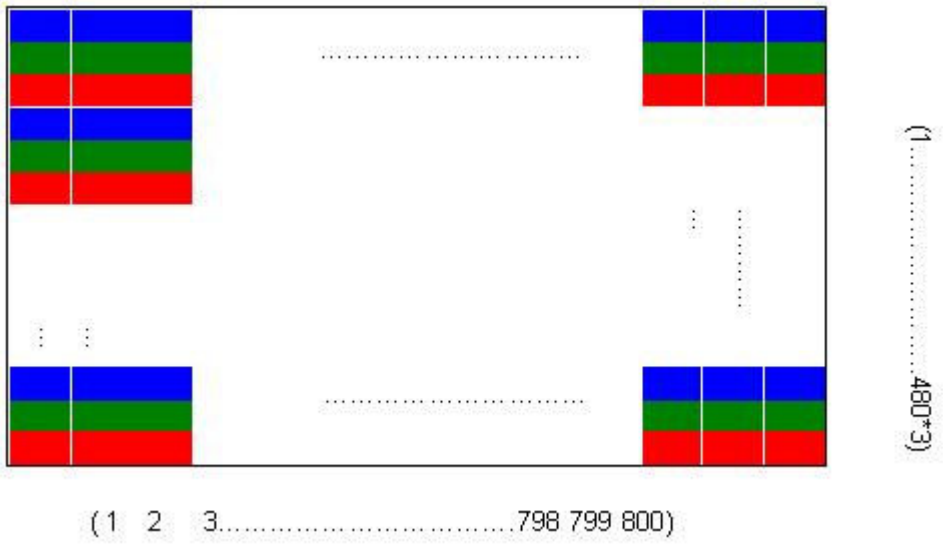
A. General Information

This product is for digital photo frame and other suitable application.

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	7(Diagonal)	
2	Display Resolution	dot	800(H)×480RGB(V)	
3	Overall Dimension	mm	164(H) × 103(V) × 5.1(T)	Note 1
4	Active Area	mm	152.40(H)×91.44(V)	
5	Pixel Pitch	mm	0.1905(H)×0.1905(V)	
6	Color Configuration	--	Tri-Gate	Note 2
7	Color Depth	--	16.7M Colors	Note 3
8	NTSC Ratio	%	50	
9	Display Mode	--	Normally White	
10	Panel surface Treatment	--	Anti-Glare, 3H	
11	Weight	g	150±10	
12	Panel Power Consumption	mW	TBD	Note 4
13	Backlight Power Consumption	W	1.8	
	Viewing direction		6 o'clock (gray inversion)	

Note 1: Not include blacklight cable and FPC. Refer next page to get further information.

Note 2: Below figure shows dot stripe arrangement.

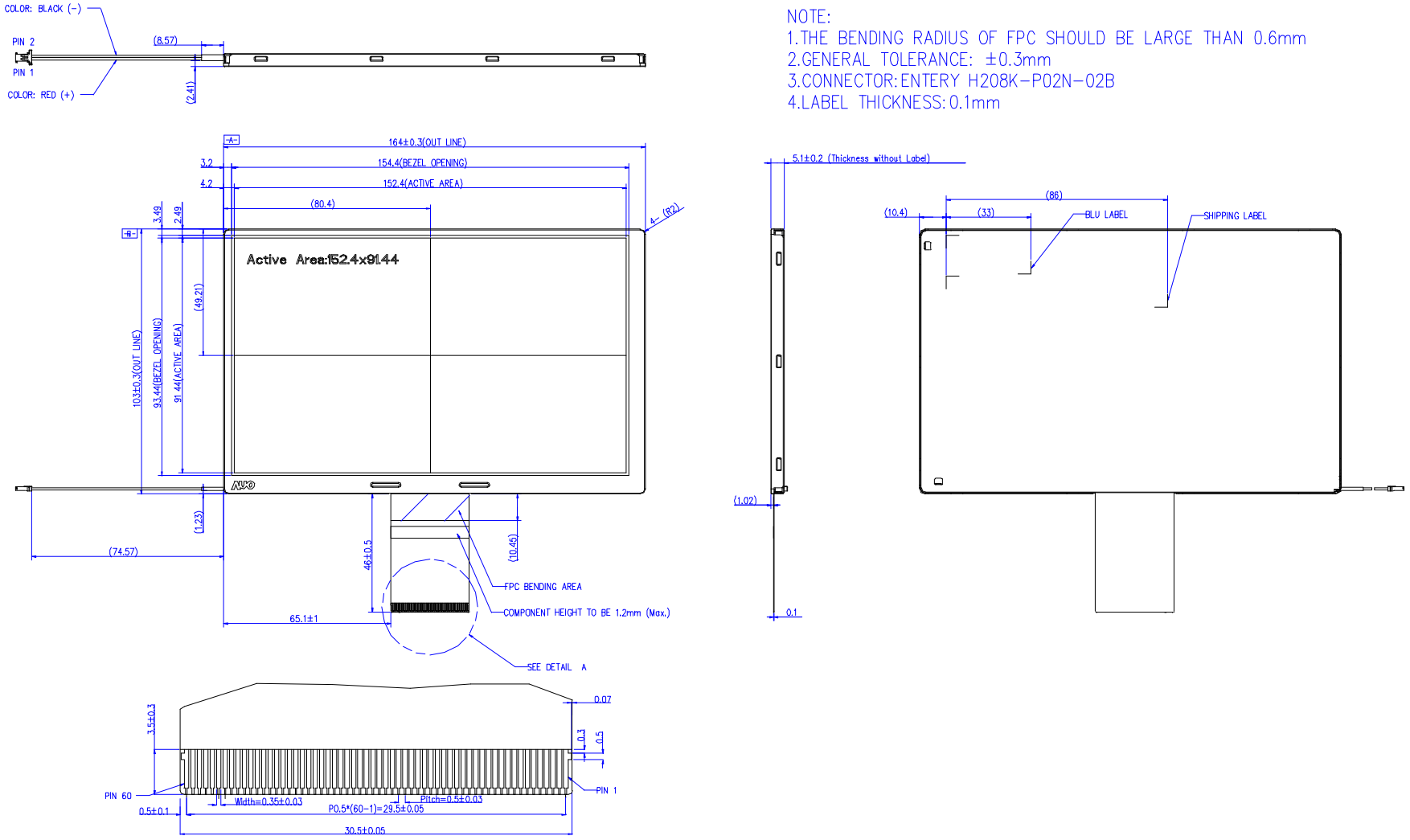


Note 3: The full color display depends on 24-bit data signal **(pin 33~40, 42~49, 51~58)**

Note 4: Please refer to Electrical Characteristics chapter.

B. Outline Dimension

1. TFT-LCD Module



NOTE:
1.THE BENDING RADIUS OF FPC SHOULD BE LARGE THAN 0.6mm
2.GENERAL TOLERANCE: ±0.3mm
3.CONNECTOR: ENTERY H208K-P02N-02B
4.LABEL THICKNESS: 0.1mm

C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector :

Pin No.	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	VGL	P	Negative power supply voltage for Gate driver	
3	VGH	P	Positive power supply voltage for Gate driver	
4	VGH	P	Positive power supply voltage for Gate driver	
5	VDPA	P	Positive Supply voltage for analog power	
6	VDNA	P	Negative Supply voltage for analog power	
7	GND	P	Ground for digital circuit	
8	DRV_BLU	O	OUTPUT_PWM_SIGNAL output via an output buffer	
9	CABC_EN	I	CABC function enable (**active high**)	
10	UD	P	Up / Down Select	Note2
11	RL	O	Right / Left Select	Note2
12	GRB	I	Global reset pin (**active low: reset when GRB='L'**)	Note1
13	V10	I	Gamma correction voltage reference	
14	V9	I	Gamma correction voltage reference	
15	V8	I	Gamma correction voltage reference	
16	V7	I	Gamma correction voltage reference	
17	V6	I	Gamma correction voltage reference	
18	V5	I	Gamma correction voltage reference	
19	V4	I	Gamma correction voltage reference	
20	V3	I	Gamma correction voltage reference	
21	V2	I	Gamma correction voltage reference	
22	V1	I	Gamma correction voltage reference	
23	**VDDIO**	P	Supply voltage for digital circuit	
24	**VDDIO**	P	Supply voltage for digital circuit	
25	CS	I	Chip select (Low active) of SPI	
26	SDA	I/O	Data input/output of SPI	
27	SCL	I	Clock input of SPI	
28	GND	P	Ground for digital circuit	
29	DCLK	I	Data clock Input	
30	GND	P	Ground for digital circuit	
31	DE	I	Data enable Input	
32	GND	P	Ground for digital circuit	

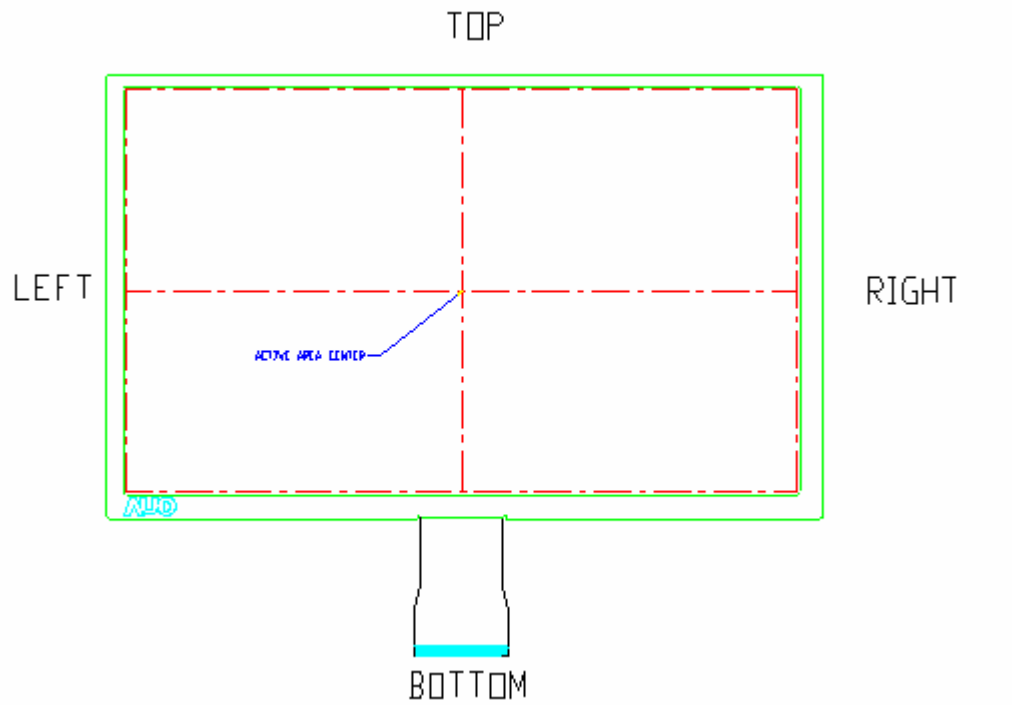
33	DB7	I	Blue data input **(MSB)**	
34	DB6	I	Blue data input	
35	DB5	I	Blue data input	
36	DB4	I	Blue data input	
37	DB3	I	Blue data input	
38	DB2	I	Blue data input	
39	DB1	I	Blue data input	
40	DB0	I	Blue data input **(LSB)**	
41	GND	P	Ground for digital circuit	
42	DG7	I	Green data input **(MSB)**	
43	DG6	I	Green data input	
44	DG5	I	Green data input	
45	DG4	I	Green data input	
46	DG3	I	Green data input	
47	DG2	I	Green data input	
48	DG1	I	Green data input	
49	DG0	I	Green data input **(LSB)**	
50	GND	P	Ground for digital circuit	
51	DR7	I	Red data input **(MSB)**	
52	DR6	I	Red data input	
53	DR5	I	Red data input	
54	DR4	I	Red data input	
55	DR3	I	Red data input	
56	DR2	I	Red data input	
57	DR1	I	Red data input	
58	DR0	I	Red data input **(LSB)**	
59	GND	P	Ground for digital circuit	
60	VCOM	I	Common electrode driving voltage	

I: Input; P: Power

Note1: Global reset, normally pulled high. Suggest to connecting with an RC (R=10K ohm, C=1uF) reset circuit for stability. Normally pull high.

Note2:

U/D	Direction	**L/R**	Direction
H	D → U	H	R → L
L	U→ D	L	L → R



2. Backlight Pin Assignment

Recommended connector :E&T H201K-P020N-02B

Pin no	Symbol	I/O	Description	Remark
1	VLED	P	LED power supply	
2	GNDLED	P	LED ground	

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VDDIO	GND=0	-0.5	5	V	
	VDPA	GND=0	-0.5	5.9	V	
	VDNA	GND=0	-5.9	0.5	V	
	VGH - VGL	GND=0	-	32	V	
Input signal voltage	Vi	GND=0	-0.3	VDDIO+0.3	V	Note 1
	VCOM	GND=0	-3.5	0		
	V1~V5	GND=0	0	VDPA-0.2		
	V6~V10	GND=0	VDNA+0.2	0		
Operating Temperature	Topa				□	
Storage temperature	Tstg				□	

Note 1:De, Digital Data

Note 2:Functional operation should be restricted under ambient temperature (25□).

Note 3:Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

4. Electrical DC Characteristics

a. (VDDIO = +3.3V, NDPA=5V,VDNA=-5V, AGND=GND=0V, TOPR = -10°C to +60°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		VDDIO	3.0	3.3	3.6	V	Digital power
		VDPA	4.5	5	5.5	V	Analog Power
		VDNA	-5.5	-5	-4.5	V	Analog Power
		VGH	13.5	14	14.5	V	Positive power supply for gate driver
		VGL	-14.5	-14	-13.5	V	Negative power supply for gate driver
Input Signal Voltage	H Level	VIH	VDDIOx0.7	TBD	VDDIO	V	Note 1
	L Level	VIL	GND	TBD	0.3xVDDIO	V	
Gamma reference voltage		VCOM		TBD		V	Detail Gamma voltage please refer to page 26 Note 2
		V1		TBD		V	
		V2		TBD			
		V3		TBD			
		V4		TBD			
		V5		TBD			
		V6		TBD			
		V7		TBD			
		V8		TBD			
		V9		TBD			
		V10		TBD			

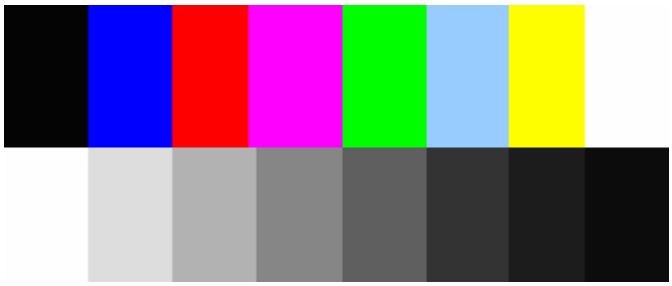
Note 1: DE , Digigal Data

Note 2: VDPA > V1 > V2 > V3 > V4 > V5 > V6 > V7 > V8 > V9 > V10 > VDNA

b. Current Consumption (AGND=GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input current for VDDIO	I_{VDDIO}	VDDIO=3.3V	-	TBD		mA	Note 1
Inpur current for VDPA	I_{VDPA}	VDPA=5V	-	TBD		mA	Note 1
Input current for VDNA	I_{VDNA}	VDNA=-5V	-	TBD		mA	Note 1
Inpur current for VGH	I_{VGH}	VGH=14V	-	TBD		mA	Note 1
Inpur current for VGL	I_{VGL}	VGL= -14V		TBD		mA	Note 1
Inpur current for VCOM	I_{VCOM}	VCOM=TBD		TBD		mA	Note 1

Note 1: The test pattern use the following pattern.

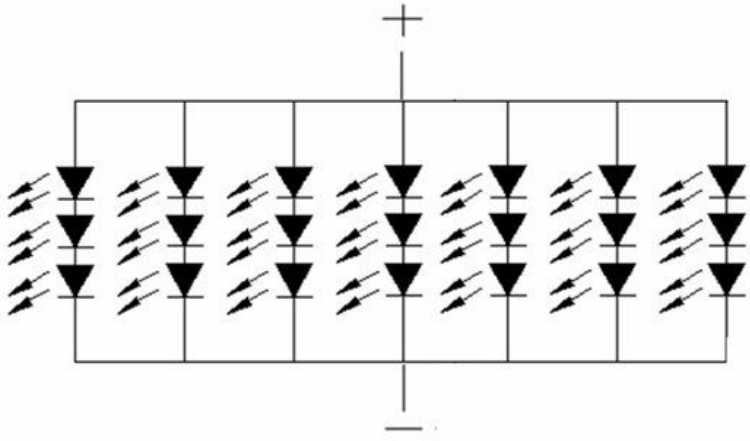


c. Backlight Driving Conditions

The backlight (LED module, Note 1) is suggested to drive by constant current 175mA.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED light bar Voltage	V_L	8.85	9.75	10.95	V	I_F=175mA
Power Consumption	P_{BL}	1.548	1.706	1.916	W	Note 1
LED Life Time	L_L	10,000	--	--	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (21 LED). The voltage range will be 8.85V to 10.95V based on suggested driving current set as 175mA.



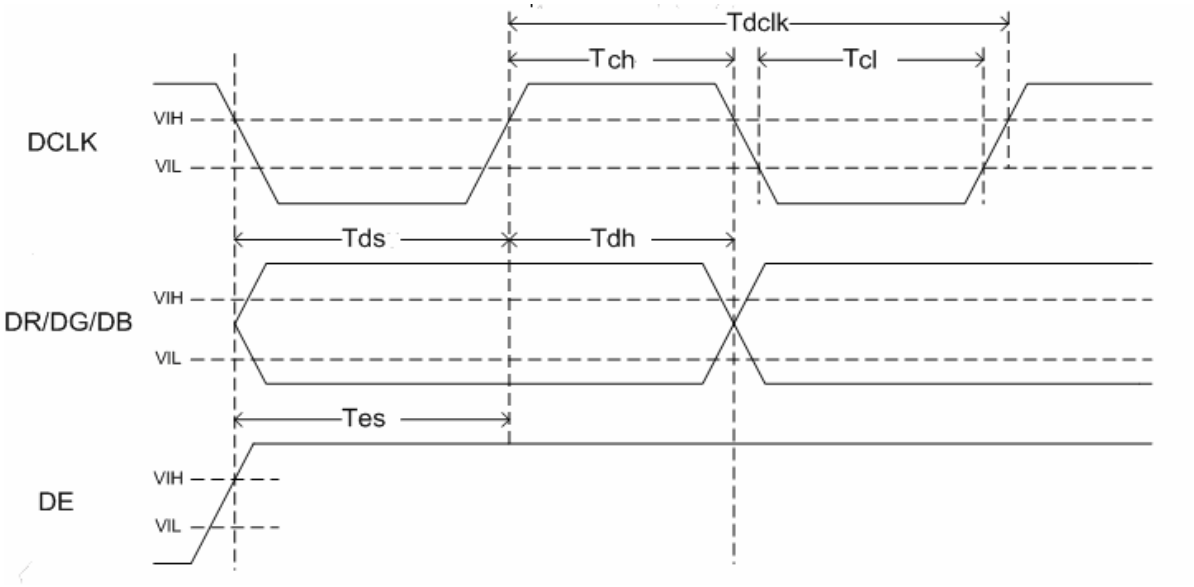
Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25□ and LED lightbar current = 175mA.

Note 3: If it uses larger LED lightbar voltage/ current more than 10.95V/175mA, it maybe decreases the LED lifetime.

5. Electrical AC Characteristics

a. Signal AC Characteristics

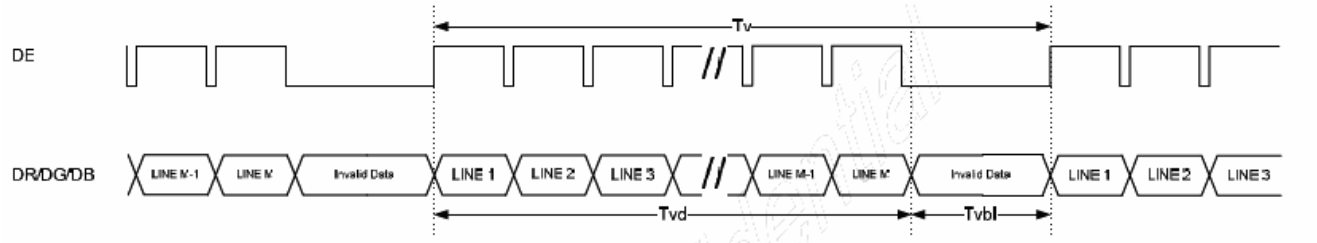
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT Signals						
Clock High time	Tch		8	-	-	ns
Clock Low time	Tcl		8	-	-	ns
Data setup time	Tds		5			ns
Data hold time	Tdh		10			ns
Data enable set-up time	Tes		4			ns



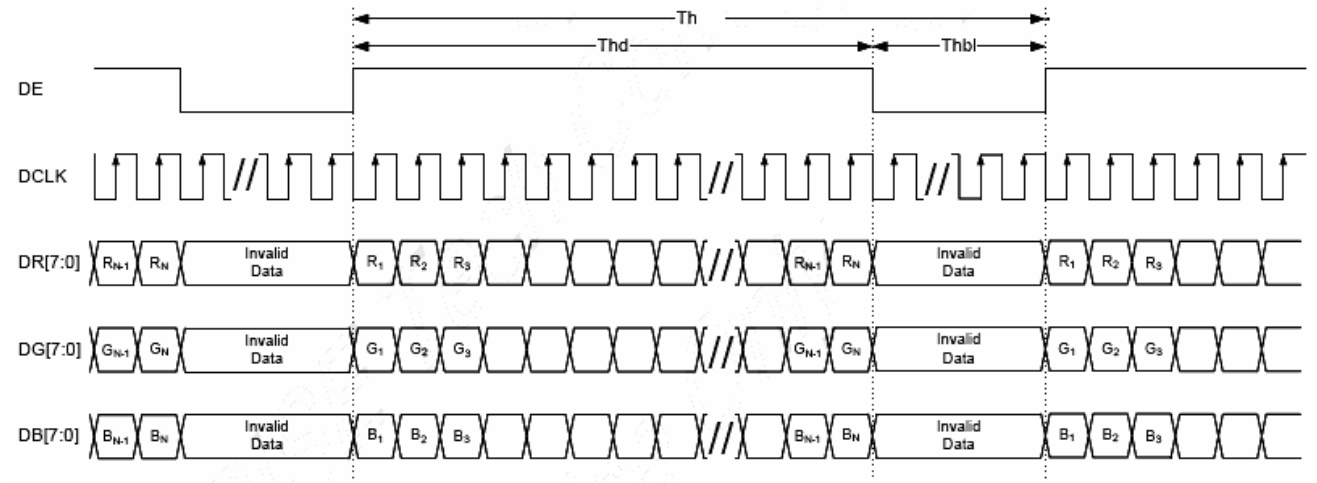
b. Input timing Setting (DE Mode only)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remark
DCLK frequency	F_{DCLK}	30.3	33.26	37.8	MHz	
Hsync period (= Thd + Thbl)	Th	986	1056	1183	T_{DCLK}	Note 1,2
Active Area	Thd	--	800	--	T_{DCLK}	
Horizontal blanking (= Thf+ The)	Thbl	186	256	383	T_{DCLK}	
Vsync period (= Tvd + Tvbl)	Tv	517	525	532	Th	
Active lines	Tvd	--	480	--	Th	
Vertical blanking (=Tvf + Tve)	Tvbl	37	45	52	Th	

Vertical timing:



Horizontal timing:



Note: horizontal resolution N = 800

Note: vertical resolution M = 480

Note 1: If input timing operates with Min. to Typ. setting, the PWCK value use default value 1973 (Register R39=0000_0111, Register R40=1011_0101), and no need to change SPI register.

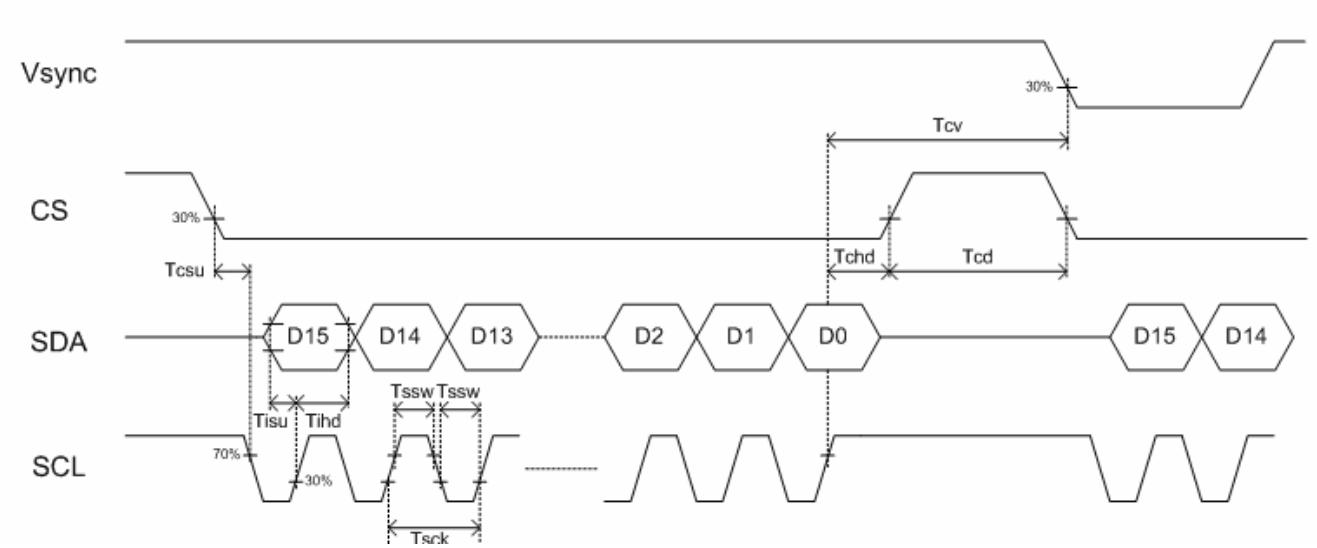
Note 2: If input timing operates with Typ. to Max. setting, the PWCK value must be set to 2025(Register R39=0000_0111, Register R40=1110_1001). Please reference the Serial interface setting table in Page.16 to set SPI Register R39 and R40 value.

6. Serial Interface Characteristics

a.Serial Control Interface

SERIAL Communication						
Serial clock	Tsck		320			ns
SCL pulse duty	Tscw		40%	50%	60%	Tsck
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
Serial clock high/low	Tssw		120			ns
CS setup time	Tcst		120			ns
CS hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay from CSB to Vsync	Tcv		1			us

AC serial interface write mode timings



b. Register Bank

A totally 16-bit register including 7-bit address D[15:9], 1-bit R/W bit D[8] and 8-bit data D[7:0] can be set via 3-wire serial peripheral interface. Below figure is for a detail description of the parameters.

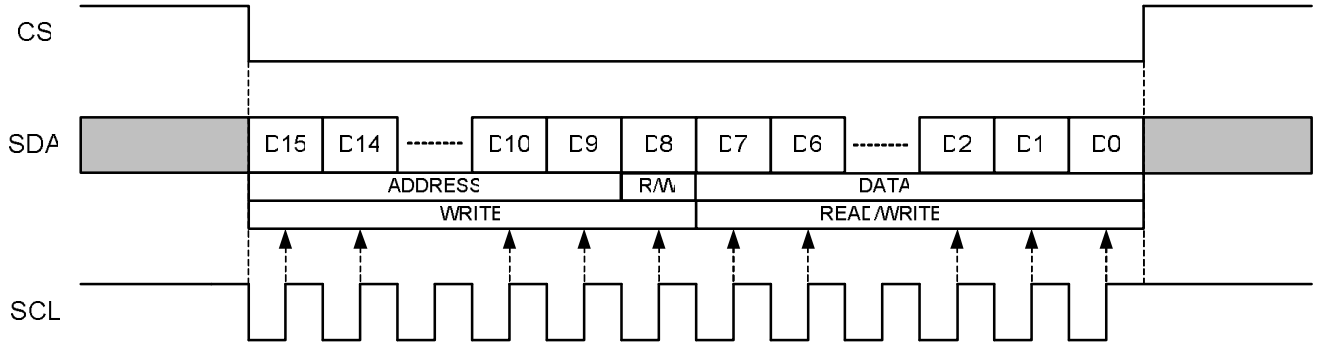


Figure: Serial interface write/read sequence

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the following the following rising edge of the End Frame(DE mode). If command is transferred multiple times for the same register, the last command before the following rising edge of the End Frame(DE mode) is valid, except for some special registers (ex. GRB, etc.).
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
  - The write operation is cancelled.
  - The read operation is interrupt.
- If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data in the duration of CS="L" are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the standby (power save) mode.
- Register R/W setting: D8 = "L" → write mode; D8 = "H" → read mode.
- It is suggested that DE,DCLK(for DE mode) always exists in the same time.

c.Serial Interface Setting Table.

Reg	ADDRESS							R	DATA							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	--	--	--	1 note 1	1 note 1	1 note 1	0	1
R1	0	0	0	0	0	0	1	0	0 note 1	0 note 1	--	--	00		00	
R39	0	1	0	0	1	1	1	0	--	--	--	--	PW_CK			
R40	0	1	0	1	0	0	0	0	PW_CK							

d.Register Description

R0 settings

Address	Bit	Discription		Default
000000	7 - 2	--	AUO internal use	000111
	1	STB	Standby mode setting	0
	0	GRB	S/W global reset	1

Bit 1	STB
0	Nomal operation **(default)**
1	Standby mode. Register data are kept.

Bit 0	GRB
0	S/W global reset. Reset all register to default value. H/W GRB has higher priority.
1	Normal operation. **(default)**

S/W GRB	H/W GRB	Operation mode
0	0	H/W reset
0	1	Execute S/W reset procedure
1	0	H/W reset
1	1	Normal operation

R1 Settings

Address	Bit	Discription		Default
000001	7 - 4	--	AUO internal use	0000
	3 - 2	CHUD	Vertical scan direction setting	00
	1 - 0	CHLR	Horizontal scan direction setting	00

Bit 3 - 2	CHUD
0x	Accoring to H/W pin U/D setting. **(default)**
10	Vertical scan direction is from up to down.
11	Vertical scan direction is from down to up.

Bit 1 - 0	CHLR
0x	Accoring to H/W pin L/R setting. **(default)**
10	Horizontal scan direction is from left to right.
11	Horizontal scan direction is from right to left.

R39 setting

Address	Bit	Discription		Default
100111	3 - 0	--	AUO PW_CK default value	0111
	3 - 0	--	AUO PW_CK Max value	0111

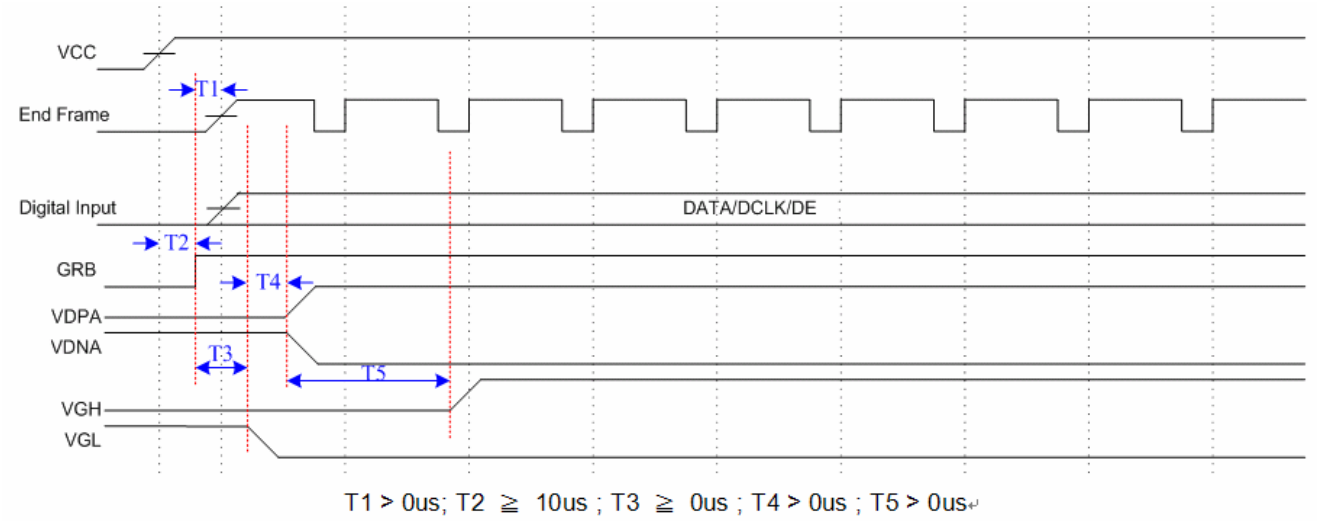
R40 setting

Address	Bit	Discription		Default
101000	7 - 0	--	AUO PW_CK default value	1011_0101
	7 - 0	--	AUO PW_CK Max value	1110_1001

7. Power On/Off Characteristics

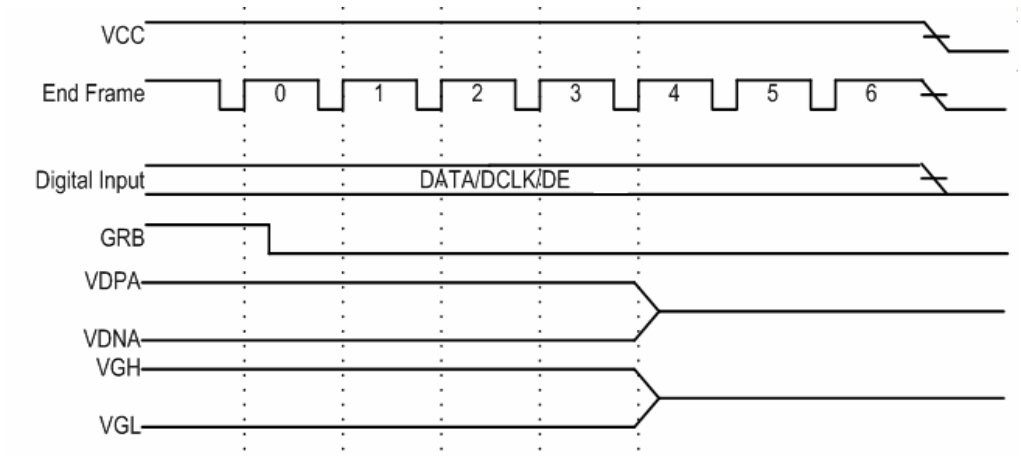
This IC may be damaged by a large current flow when an incorrect power sequence is applied. The recommended power-on sequence is to first connect the logical power (VDDIO=VCC&GND), then the digital signal (DCLK,DE), and then the global reset (GRB). After GRB rise up, five frames time is necessary and then the VGL is produced. Finally, VDPA,VDPA and VGH are produced. Under the power on sequence, panel can normally start up.

a. Recommended Power On Register Setting



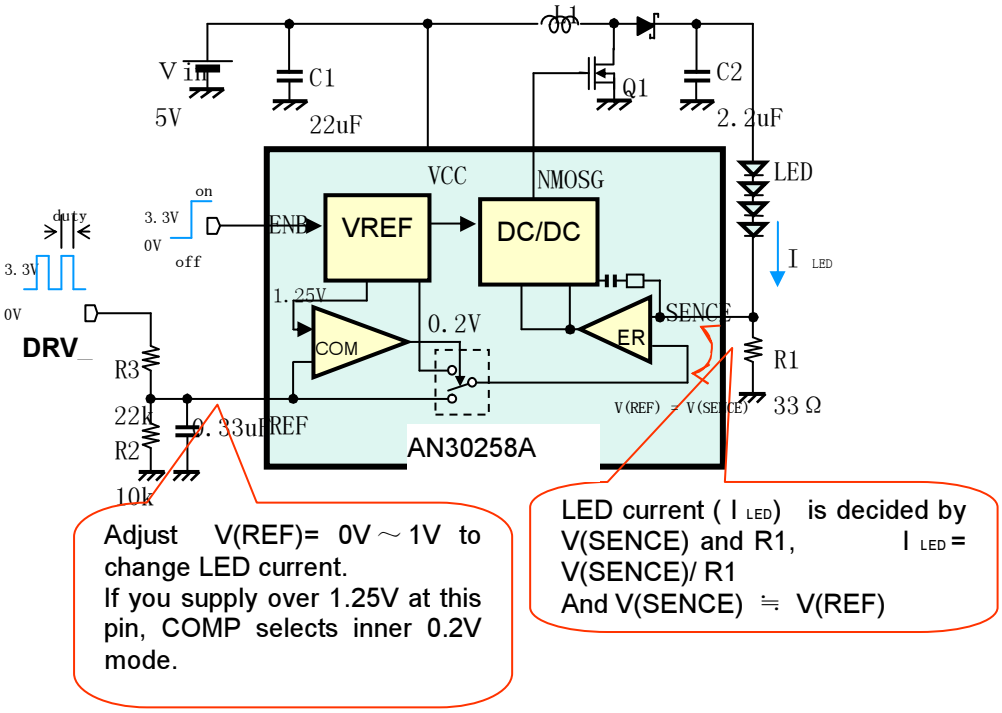
T1 > 0us; T2 ≧ 10us ; T3 ≧ 0us ; T4 > 0us ; T5 > 0us

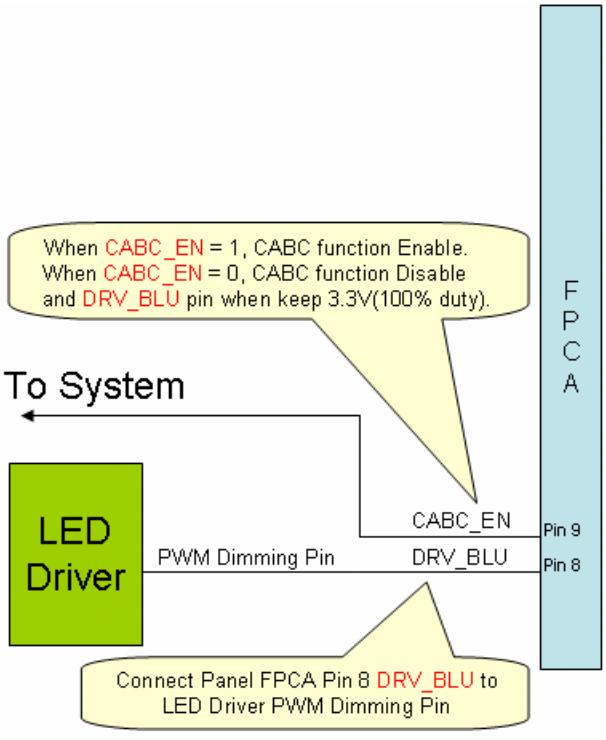
b. Recommended Power Off Sequence



8. Content-based Automatic Backlight Control (CABC) reference circuit

It is used in a step-up DCDC converter that drives an external NMOS power transistor using a constant frequency PWM architecture. With 2 current modes (Dimmi Mode / Normal Mode) selectable.





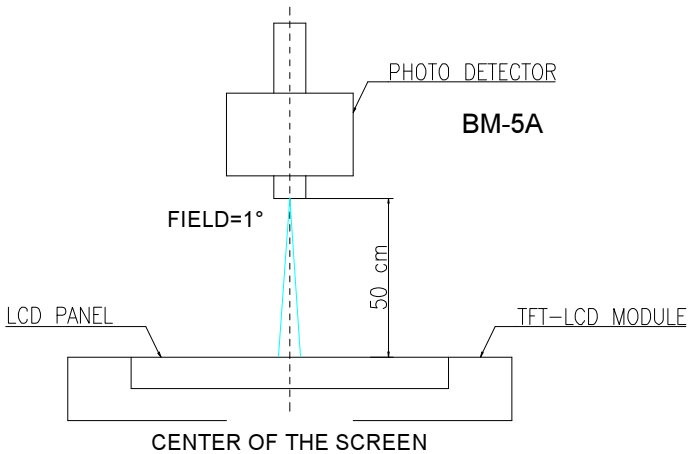
D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 12 18	 20 30	 ms ms	Note 3
Contrast ratio		CR	At optimized viewing angle		500	--		Note 4
Viewing Angle	Top Bottom Left Right		CR□10	40 50 55 55	50 60 65 65		deg.	Note 5
Brightness		Y_L	θ=0°		250	--	cd/m^2	Note 6
Chromaticity	White	X	θ=0°	0.25	0.30	0.35		
		Y	θ=0°	0.27	0.32	0.37		
	Red	X	θ=0°		TBD			
		Y	θ=0°		TBD			
	Green	X	θ=0°		TBD			
		Y	θ=0°		TBD			
	Blue	X	θ=0°		TBD			
		Y	θ=0°		TBD			
Uniformity		ΔY_L	%	70	75	--	%	Note 7

Note 1: Ambient temperature =25□, and LED lightbar current:175mA. To be measured in the dark room.

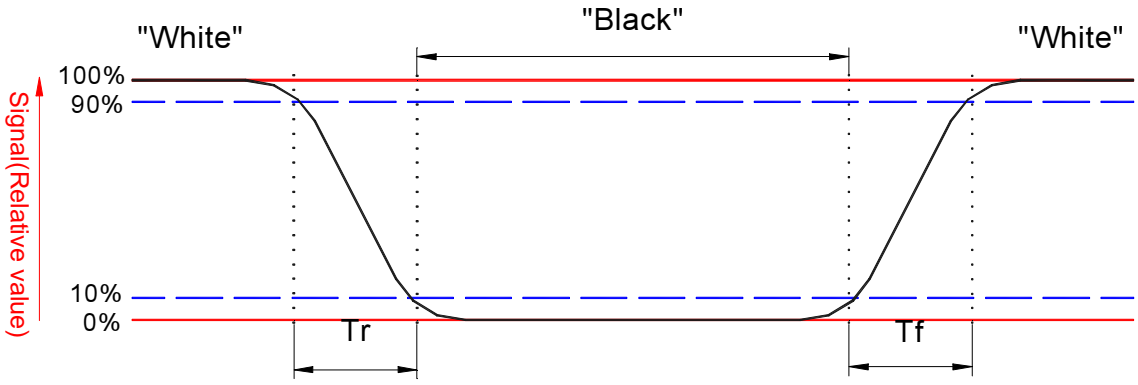
Note 2: To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-5A, after 15 minutes operation.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

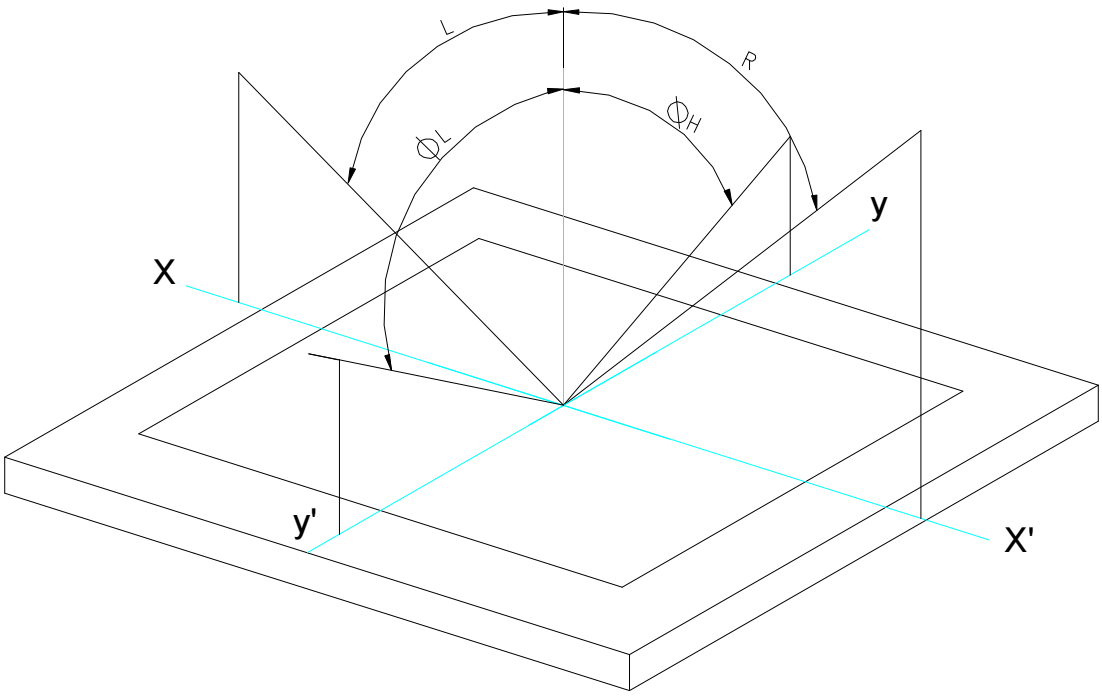


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

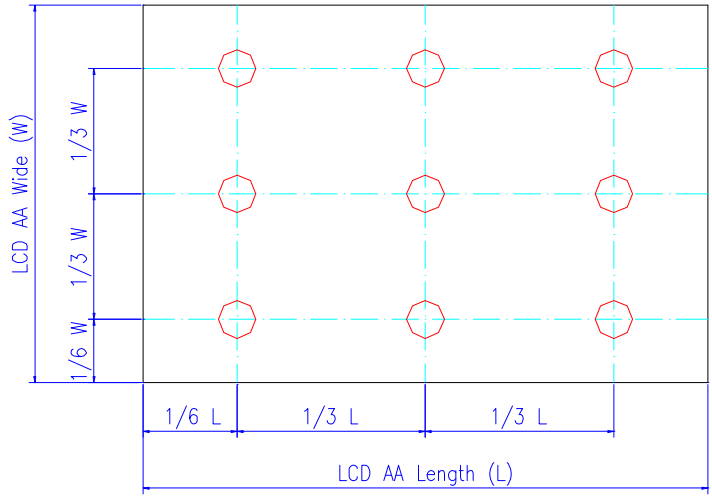
$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" status}}{\text{Photo detector output when LCD is at "Black" status}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 7: Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

E. Reliability Test Items

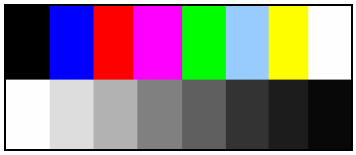
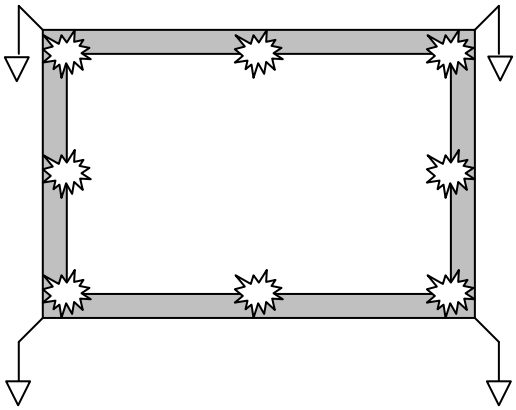
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -20□ 240Hrs	
3	High Ttemperature Operation	Tp=60□ 240Hrs	
4	Low Temperature Operation	Ta= -10□ 240Hrs	
5	High Temperature & High Humidity	Tp= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-20□~70□, 50 cycle, 0.5Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	
8	Image Sticking	25□, TBD	Note 5
9	Vibration	Frequency range : 10Hz~55Hz Stoke : 1.5mm Sweep : 10Hz~55Hz~10Hz 2 hours for each direction of X,Y,Z. Total 6 hours.	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
13	Pressure	5kg, 5sec	Note 6

Note 1: Ta: Ambient Temperature. Tp: Panel Surface Temperature

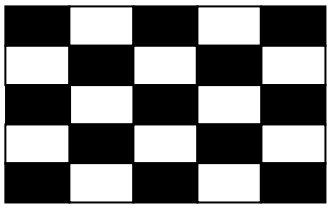
Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 3: All the cosmetic specification is judged before the reliability stress.

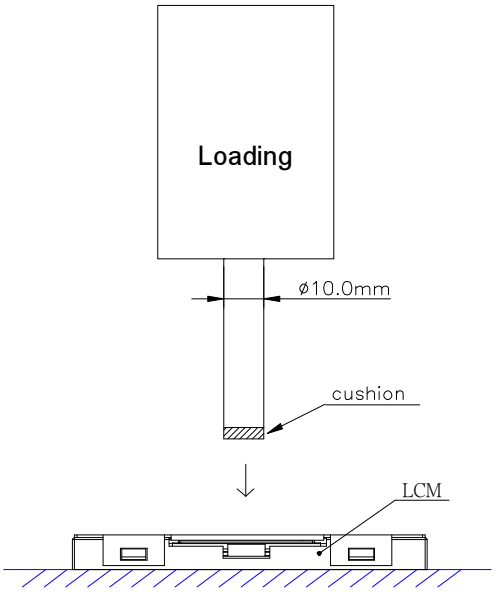
Note4 : All test techniques follow IEC6100-4-2 standard.

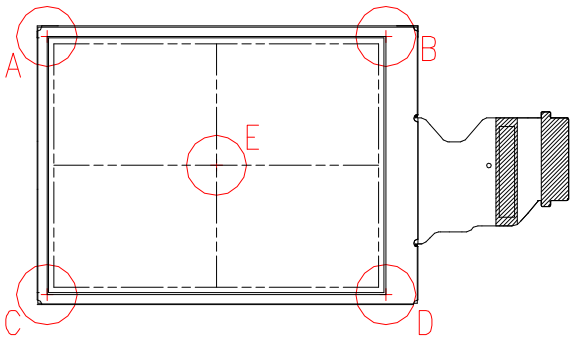
Test Condition		Note
Pattern		
Procedure And Set-up	Contact Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point Air Discharge：330Ω, 150pF, 1sec, 8 point, 25times/point 	
Criteria	B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Gun to Panel Distance 2. No SPI command, keep default register settings.	

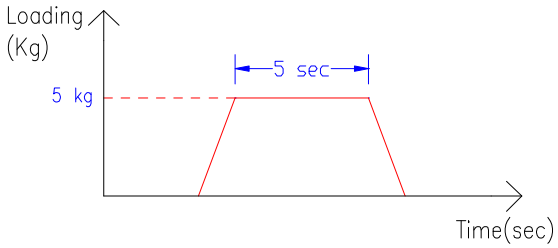
Note 5: Operate with 5 x 5 chess board pattern as figure and lasting time and temperature as the conditions. Then judge with 32 degree gray pattern, the mura is less than JND 2.5



Note 6: The panel is tested as figure. The jig isψ10 mm made by Cu with rubber and the loading speed is 3mm/min on position A~E. After the condition, no glass crack will be found and panel function check is OK.(no guarantee LC mura、LC bubble)

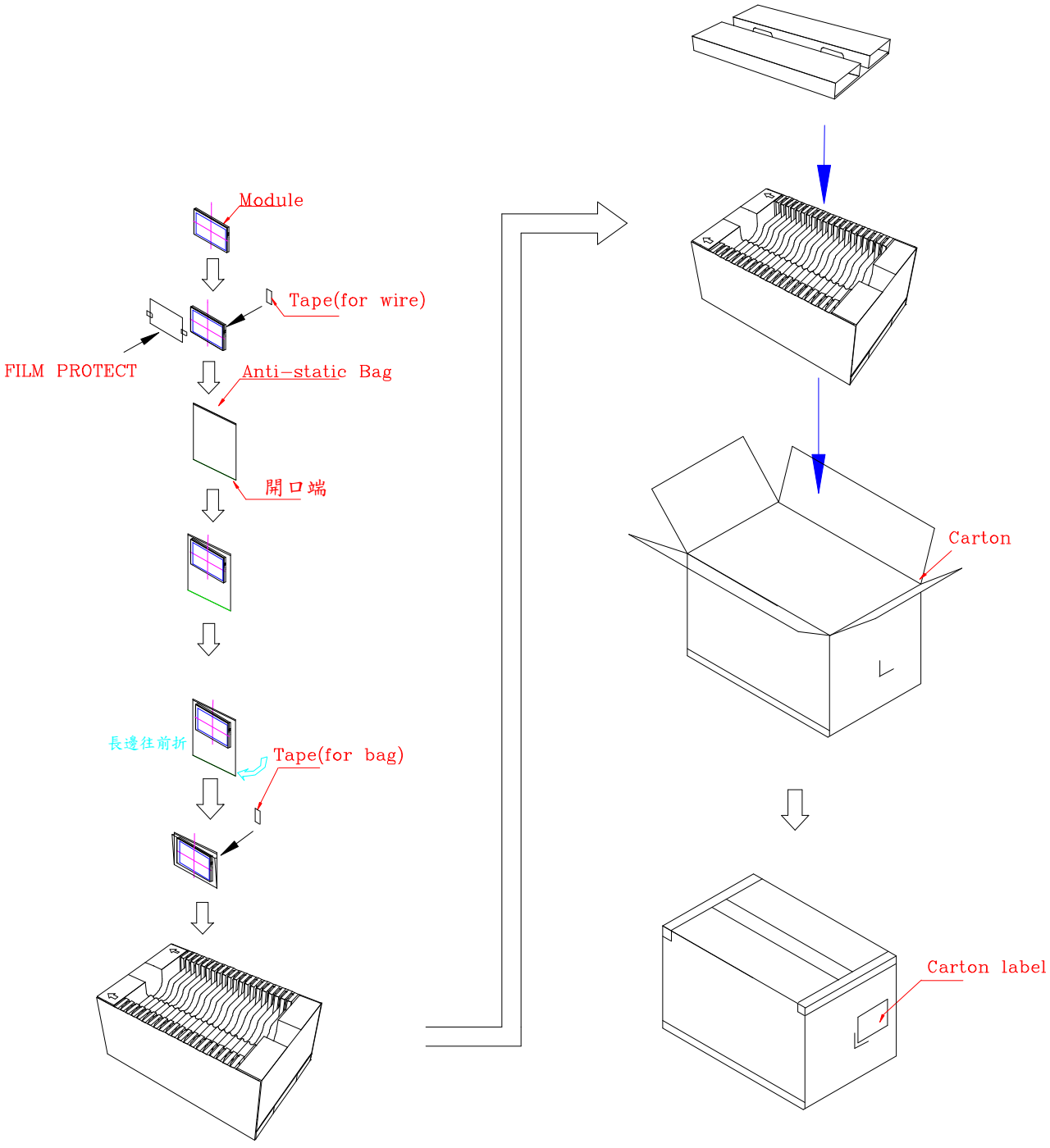






F. Packing and Marking

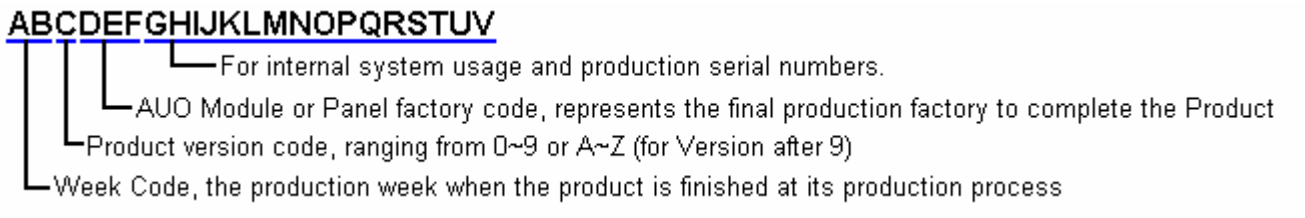
1. Packing Form



Max. Capacity: 40 Pcs Modules
Carton outline.: 520mm*340mm*250mm

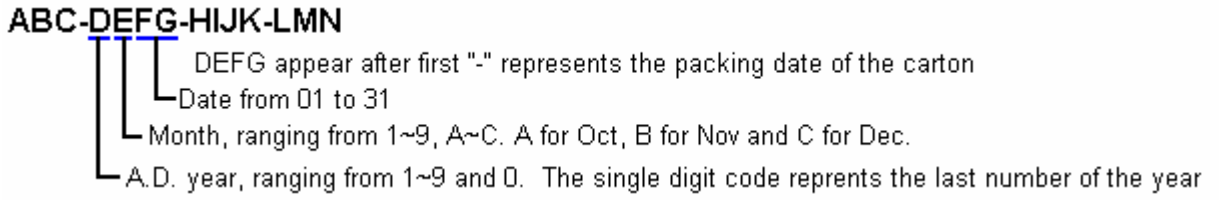
2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:



3. Carton Label Information

The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:



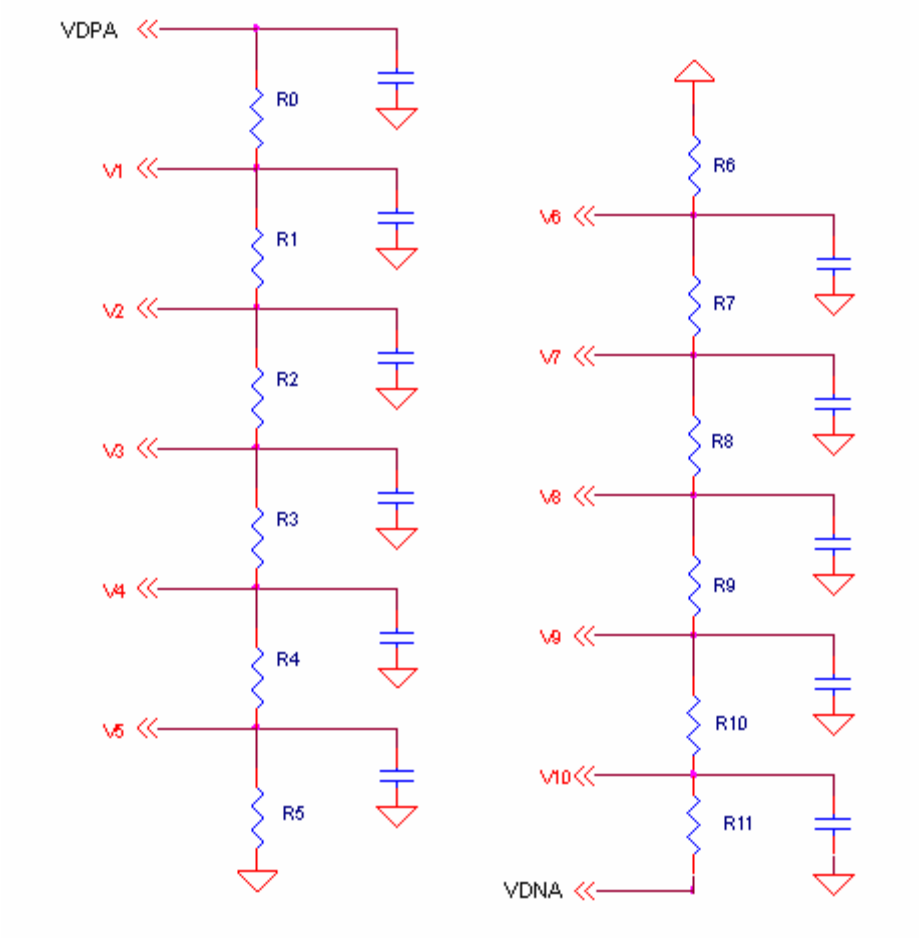
Refer to the drawing of packing format for the location and size of the carton label.

G. Reference application circuit

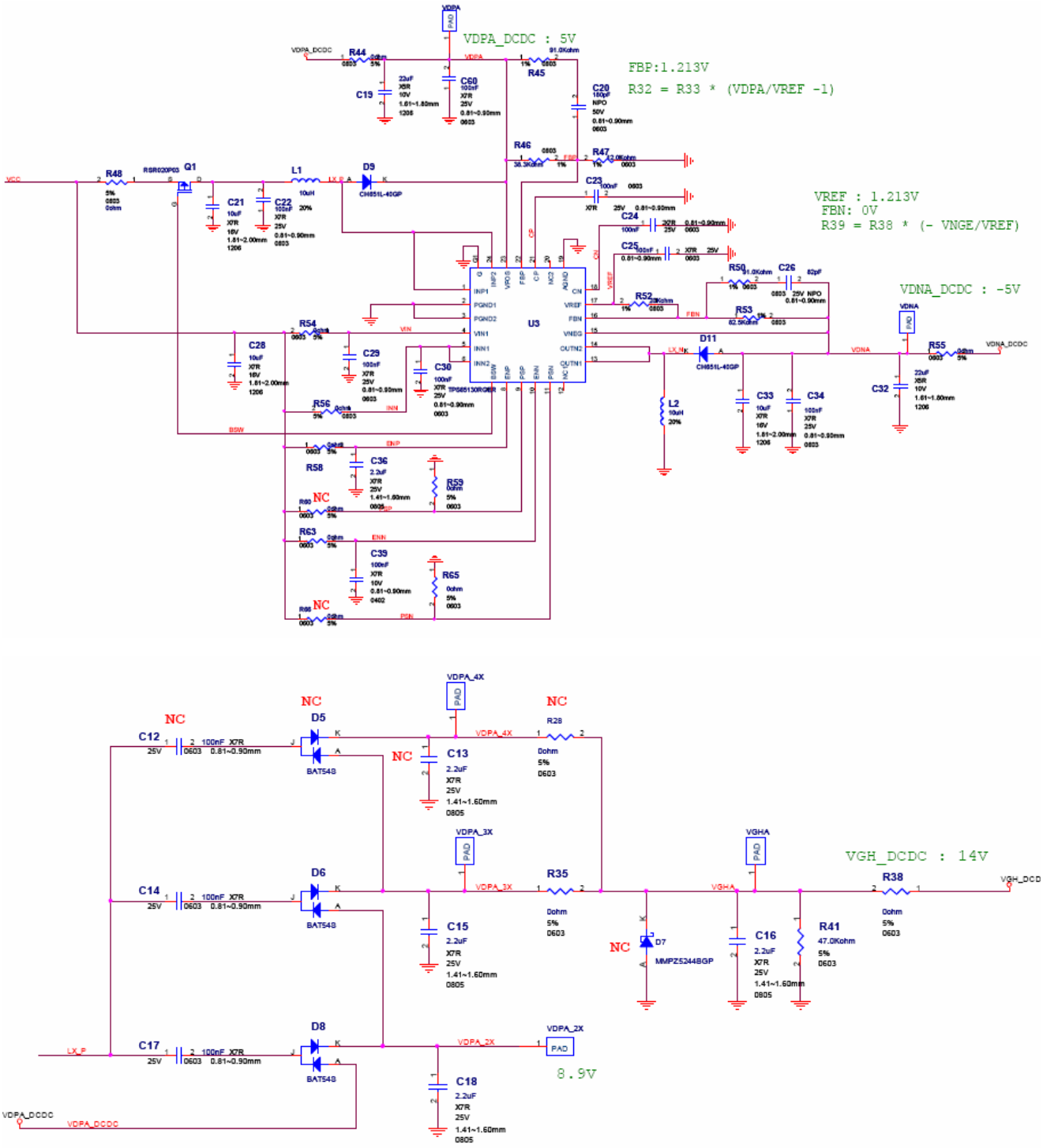
1. Recomonded Gamma Voltage

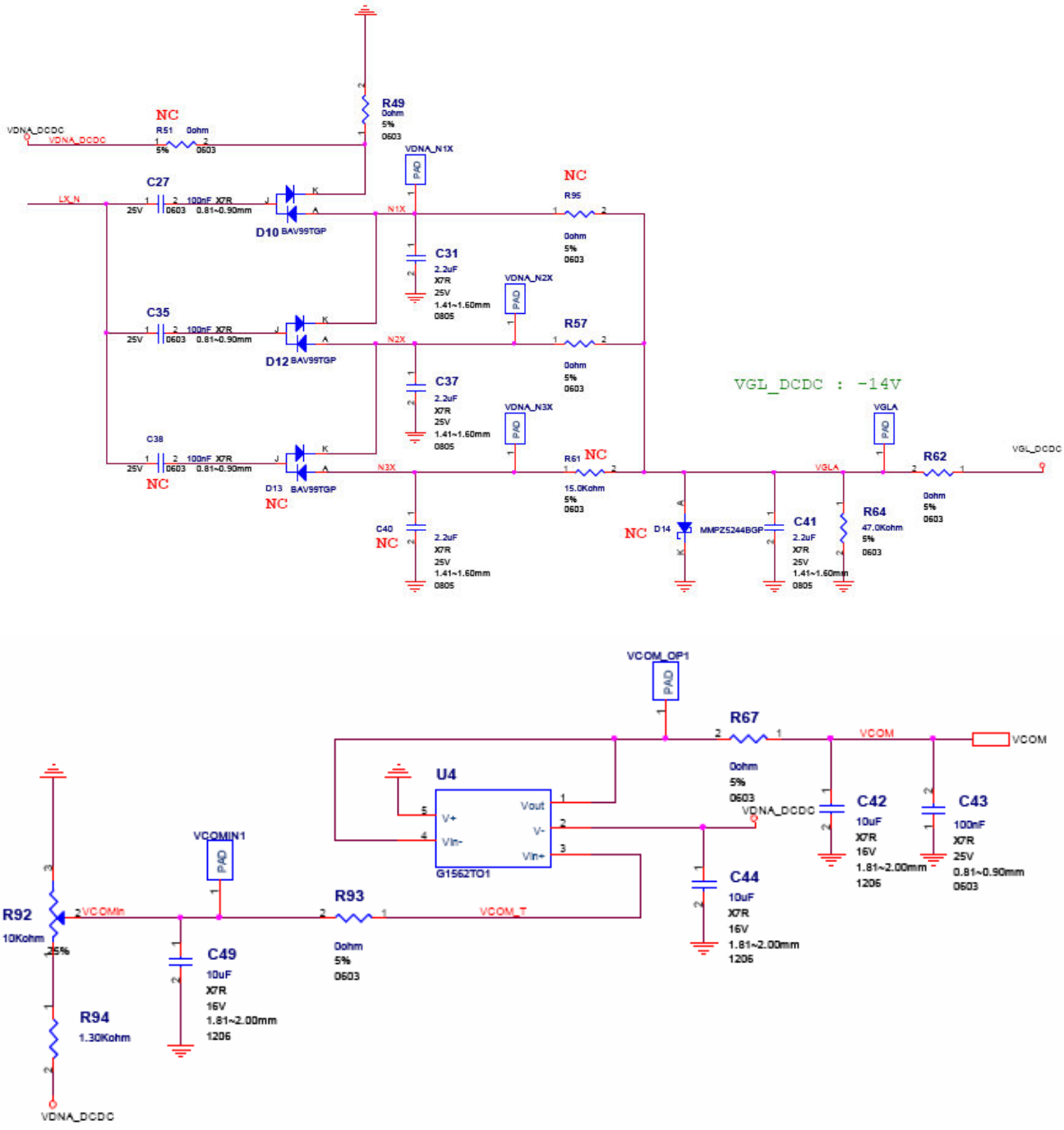
Symbol	Value (V)
V1	TBD
V2	TBD
V3	TBD
V4	TBD
V5	TBD
V6	TBD
V7	TBD
V8	TBD
V9	TBD
V10	TBD
VDPA	+5
VDNA	-5
VCOM	TBD

:



2. Application Circuit





H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.